



International Journal of Multidisciplinary Research in Science, Engineering and Technology

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)



Impact Factor: 8.206

Volume 9, Issue 3, March 2026



International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Design and Verification of UART Serial Communication

G.Yeshoda¹, D. Sai Kumar², T.Kavya³, P.Jyothi⁴

U.G. Student, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India^{1,2,3}

Assistant Professor, Department of ECE, SVIET Engineering College, Nandamuru, Pedana, Andhra Pradesh, India⁴

ABSTRACT: In the contemporary landscape of semiconductor design, the complexity of System-on-Chip (SoC) architectures has escalated exponentially, necessitating robust and scalable verification methodologies. As integrated circuits integrate billions of transistors, the verification gap—the disparity between design capacity and verification capability—has become a critical bottleneck. The Universal Asynchronous Receiver-Transmitter (UART) protocol, despite being a legacy standard for serial communication, remains a ubiquitous component in modern SoCs for debug interfaces, low-speed communication, and peripheral integration. This project introduces a coverage-driven verification environment for a UART Controller using UVM (Universal Verification Methodology). The design uses SystemVerilog and adopts an object-oriented, modular approach to create a reusable and scalable testbench. The environment separates verification from the design under test (DUT), enabling constrained random testing, automated checking, and functional coverage. This project is built using SystemVerilog (IEEE 1800) and follows UVM 1.2 standards. It utilizes UVM components such as test, environment, agent, driver, monitor, sequencer, and scoreboard to maintain a structured verification flow. Simulation and waveform analysis are performed using standard EDA tools like QuestaSim, VCS, or Xcelium. The system is designed to be portable across Windows and Linux platforms.

KEYWORDS: Universal Asynchronous Receiver Transmitter (UART), Universal Verification Methodology (UVM), Design Under Test (DUT), SystemVerilog, QuestaSim.

I. INTRODUCTION

In digital systems, communication between devices is very important for data transfer. One of the mostly used methods for this purpose is the Universal Asynchronous Receiver Transmitter (UART). UART is a simple and cost-effective serial communication protocol that transmits data bit by bit without using a common clock signal, making it suitable for embedded systems and microcontrollers. Although UART is simple in design, proper verification is necessary to ensure that data is transmitted and received correctly. Traditional testing methods are not sufficient to cover all possible cases and may miss errors. To solve this problem, advanced verification techniques like Universal Verification Methodology (UVM) are used.

In this project, a UART transmitter and receiver are designed using SystemVerilog. A UVM-based verification environment is developed to test the functionality of the UART module. The environment uses components such as driver, monitor, sequencer, and scoreboard to perform automated testing and checking.

Different test scenarios are applied to verify the system, including random data transmission and corner cases. The simulation results show that the transmitted data and received data are the same, which confirms the correct operation of the UART module. This project demonstrates that UVM is an effective method for verifying communication protocols and helps in building reliable and reusable verification systems.

II. RELATED WORK

Several research works have been carried out in the field of UART design and verification using different methodologies. Earlier approaches mainly focused on directed testing using Verilog testbenches, where specific input patterns were manually applied to verify the functionality of the UART module. Although these methods are simple, they are not efficient in covering all possible scenarios and may fail to detect corner-case errors. With the advancement of SystemVerilog, Constrained Random Verification (CRV) became popular for improving test coverage. In this



International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

approach, random inputs are generated within defined constraints, allowing the detection of unexpected bugs. However, managing large test environments using CRV alone becomes complex without a structured methodology.

Recent studies have emphasized the use of Universal Verification Methodology (UVM) for UART verification. UVM provides a standardized framework with reusable components such as drivers, monitors, sequencers, and scoreboards. Many research papers have demonstrated that UVM-based environments significantly improve verification efficiency, reusability, and scalability compared to traditional methods.

Some works also explored loopback testing techniques, where the transmitter output is connected to the receiver input to validate data integrity. While this approach simplifies testing, it may not always detect design errors if both transmitter and receiver share the same flaw.

In this project, a UVM-based verification environment is developed with a modular architecture and automated checking mechanism. Compared to existing methods, this approach provides better coverage, improved debugging capability, and a clear separation of components, making it more suitable for modern verification requirements.

III. METHODOLOGY

The proposed methodology used in this project is based on the Universal Verification Methodology (UVM), which provides a structured and reusable approach for verifying digital designs. The overall process includes design implementation, verification environment development, stimulus generation, and result analysis. Initially, the UART module is designed using SystemVerilog. The design consists of a transmitter and a receiver that follow standard UART protocol with one start bit, eight data bits, and one stop bit. The transmitter converts parallel data into serial form, while the receiver reconstructs the serial data back into parallel form.

To verify the functionality of the UART module, a UVM-based testbench is developed. The verification environment includes key components such as driver, monitor, sequencer, agent, and scoreboard. The driver sends input transactions to the design, while the monitor observes the output signals and converts them back into transaction-level data. The scoreboard compares the transmitted data with the received data to ensure correctness.

Constrained random verification techniques are used to generate different input scenarios automatically. This helps in testing various conditions, including normal data transmission and corner cases. Functional coverage is also used to measure how thoroughly the design has been tested.

Finally, simulation is performed using standard tools, and waveform analysis is carried out to validate the results. The methodology ensures that the transmitted data matches the received data, confirming the correct operation of the UART module.

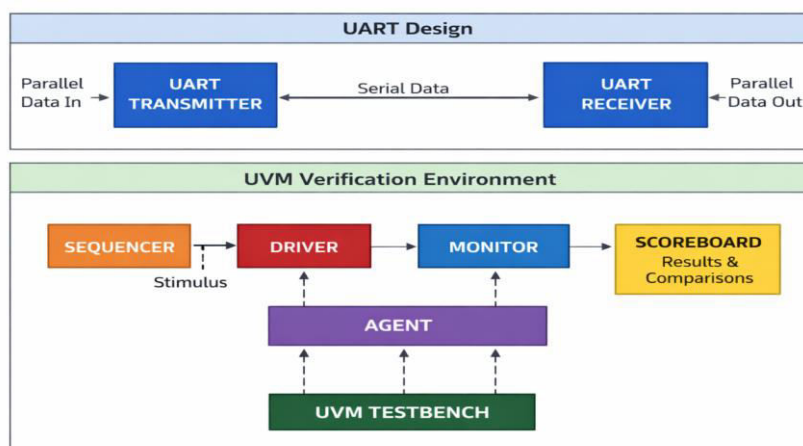


FIG 1: BLOCK DIAGRAM OF DESIGN AND VERIFICATION OF UART SERIAL COMMUNICATION



International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

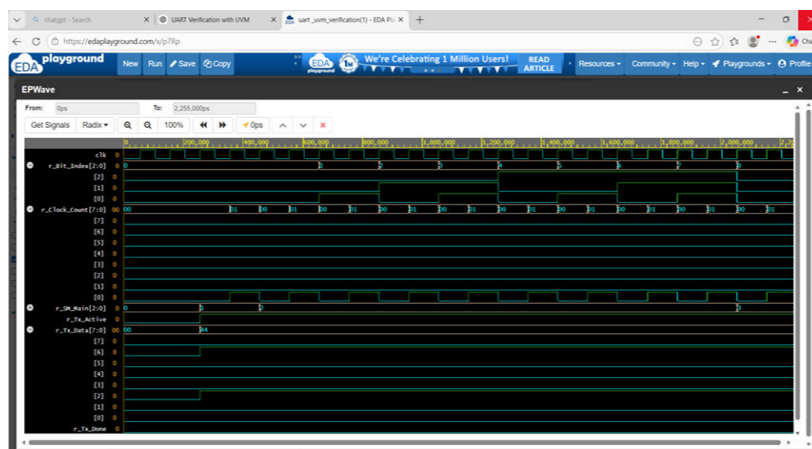
The block diagram represents the overall design and verification flow of the UART serial communication system. It is divided into two main parts: the UART design and the UVM-based verification environment. The UART design consists of a transmitter and a receiver, where the transmitter converts parallel input data into serial form, and the receiver converts the serial data back into parallel output. The serial data line connects both modules, enabling communication between them. The verification environment is built using Universal Verification Methodology (UVM), which provides a structured approach to testing. The sequencer generates stimulus in the form of transaction data, which is passed to the driver. The driver converts these transactions into signal-level inputs and applies them to the UART transmitter through the interface.

The monitor continuously observes the output signals from the design, particularly the serial data stream, and converts them back into transaction-level data. These observed transactions are then sent to the scoreboard, which compares the transmitted data with the received data to verify correctness. The agent acts as a container that groups the driver, monitor, and sequencer, making the environment modular and reusable. All these components are controlled by the UVM testbench, which manages simulation phases and execution flow.

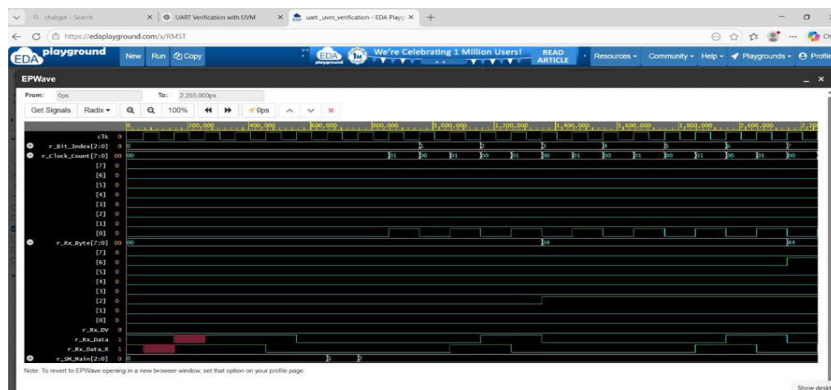
IV. EXPERIMENTAL RESULTS

The UART design and its UVM-based verification environment were successfully implemented and simulated using EDA Playground. The simulation results were analyzed using waveform viewers, which clearly show the behavior of both transmitter and receiver modules during data communication.

Fig 2:



(a) Transmitter Section Output Waveform



(b) Receiver Section Output Waveform



International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

Fig 2 shows the results of Design and Verification of UART Serial Communication (a) Transmitter section Output Waveform, (b) Receiver Section Output Waveform.

V. CONCLUSION

The project “Design and Verification of UART Serial Communication Module using UVM” has been successfully completed by implementing both the UART transmitter and receiver along with a robust UVM-based verification environment. The design correctly performs serial communication by transmitting and receiving data using standard UART protocol with proper Start bit, Data bits, and Stop bit handling. The use of Universal Verification Methodology (UVM) enabled a structured, reusable, and scalable verification approach. Through constrained random testing, functional coverage, and automated checking using the scoreboard, the verification process ensured high reliability and correctness of the design. The waveform results clearly demonstrate that the transmitted data matches the received data, confirming data integrity and proper functionality of the system.

REFERENCES

- [1] N. R. Laddha, A. P. Thakare, “Implementation of serial communication using UART with configurable baud rate,” International Journal on Recent and Innovation Trends in Computing and Communication, vol.1, Issue 4, pp. 263-268.
- [2] S. Saha, M. A. Rahman, A. Thakur, “Design and Implementation of a BIST Embedded High Speed RS- 422 Utilized UART over FPGA,” Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT), pp. 1-5, 4-6 July 2013
- [3] G. Bandhawarkar Wakhele, I. Aggarwal and S. Gaba, “Synthesis and Implementation of UART using VHDL codes,” International Symposium on Computer, Consumer and Control (IS3C), pp. 1-3, 4-6 June 2012.
- [4] F. Yi-yuan, C. Xue-jun, “Design and Simulation of UART Serial Communication Module Based on VHDL,” 3rd International workshop on Intelligent System and Applications (ISA), pp. 1-4, 28-29 May 2011.
- [5] Y. Daniel Sukumar, J. Jayanth Kumar, N. Prasad Reddy, S. David Dhinakaran, “8-BIT UART IMPLEMENTATION IN FPGA WITH BIST TECHNIQUE,” IJERSS, vol. 1, Issue 4, April 2014.
- [6] N. Patel, V. Patel, V. Patel, “VHDL Implementation of UART with Status Register,” International Conference on Communication System and Network Technologies (CSNT), pp. 750-754, 11-13 May 2012.
- [7] N. F. Mahat, “Design of a 9-bit UART Module Based on Verilog HDL,” 10th IEEE International Conference on Semiconductor Electronics (ICSE), pp. 570-573, 2012.
- [8] Y. Wang, K. Song, “A New Approach to Realize UART,” International Conference on Electronic and Mechanical Engineering and Information Technology (EMEIT), vol.5, pp.2749-2752, 12-14 Aug. 2011.



INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA



INTERNATIONAL JOURNAL OF MULTIDISCIPLINARY RESEARCH IN SCIENCE, ENGINEERING AND TECHNOLOGY

| Mobile No: +91-6381907438 | Whatsapp: +91-6381907438 | ijmrset@gmail.com |

www.ijmrset.com